Topographical and area selectivity in atomic layer deposition

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The patterning of materials is widespread in the fabrication of microelectronic and optoelectronic devices. Current patterning methods based upon bottom-up processing require many steps consisting of deposition and etching which makes the process time-consuming and expensive. In contrast, selective deposition of the desired materials has the potential to revolutionize the fabrication process and significantly reduce process complexities associated with 2-D and 3-D pattern development.

In this presentation, we will describe area selective deposition using a variety of strategies built upon atomic layer deposition (ALD). ALD is a good choice for selective deposition because it is based on self-limiting reactions between gas phase precursors and specific functional groups at the growth surface. This chemical specificity provides a means to achieve selectivity in ALD on a spatially patterned substrate. Typically, in area selective ALD, self-assembled monolayers (SAMs) are used to passivate the surface, using SAMs in the regions where deposition is not desired. For example, we will show that both alkanethiol and alkylphosphonic acid SAMs can prevent deposition of metal oxide dielectric films via ALD on copper. However, a major challenge is that after a finite amount of material is deposited, the selectivity degrades because the ALD process begins to nucleate on the regions of the surface covered with the SAM. We will describe several strategies to overcome the growth on the SAM and achieve significantly higher selectivity. In one approach, to improve the blocking properties of the SAM on copper surfaces, SAM molecules are re-dosed between ALD cycles with the purpose of recovering the SAM [1]. Results show that selectivity can be retained for much thicker deposited films. In a second strategy, a self-correcting process is applied by combining area selective ALD with selective etching of residual dielectric film, again greatly improving the final selectivity [2]. With both approaches, selective ALD of more than 60 nm of metal oxide dielectric material can be achieved.

Although 2-D patterns are important in electronic device fabrication, many applications require use of materials that are patterned into 3-D shapes. For example, in electronic devices, 3-D structures such as those found in FinFETs are becoming more prevalent. To achieve such complex structures with nanometer-scale feature sizes, we introduce a third strategy that enables topographically selective ALD. In this approach. the substrate surface is modified by ion implantation of fluorocarbons. We show that through this process, a thin (~1.5 nm) hydrophobic fluorocarbon layer is formed, which in turn causes significant retardation of nucleation during ALD. We apply the process to 3D structures, demonstrating that this method can achieve selective anisotropic deposition, selectively inhibiting Pt deposition on deactivated horizontal regions while ensuring that only vertical surfaces are decorated during ALD [3]. Future directions in area selective ALD will also be discussed.

[1] F. S. Minaye Hashemi and S. F. Bent, Adv. Mater. Interfaces, 1600464 (2016) 10.1002/admi.201600464.
[2] F. S. Minaye Hashemi, C. Prasittichai, and S. F. Bent, ACS Nano, 9 (2015) 8710–8717, 10.1021/acsnano.5b03125.
[3] W. H. Kim, F. S. Minaye Hashemi, A. J. M. Mackus, J. Singh, Y. Kim, D. Bobb-Semple, Y. Fan, T. Kaufman-Osborn, L. Godet, and S. F. Bent, ACS Nano, 10 (2016) 4451–4458, 10.1021/acsnano.6b00094.

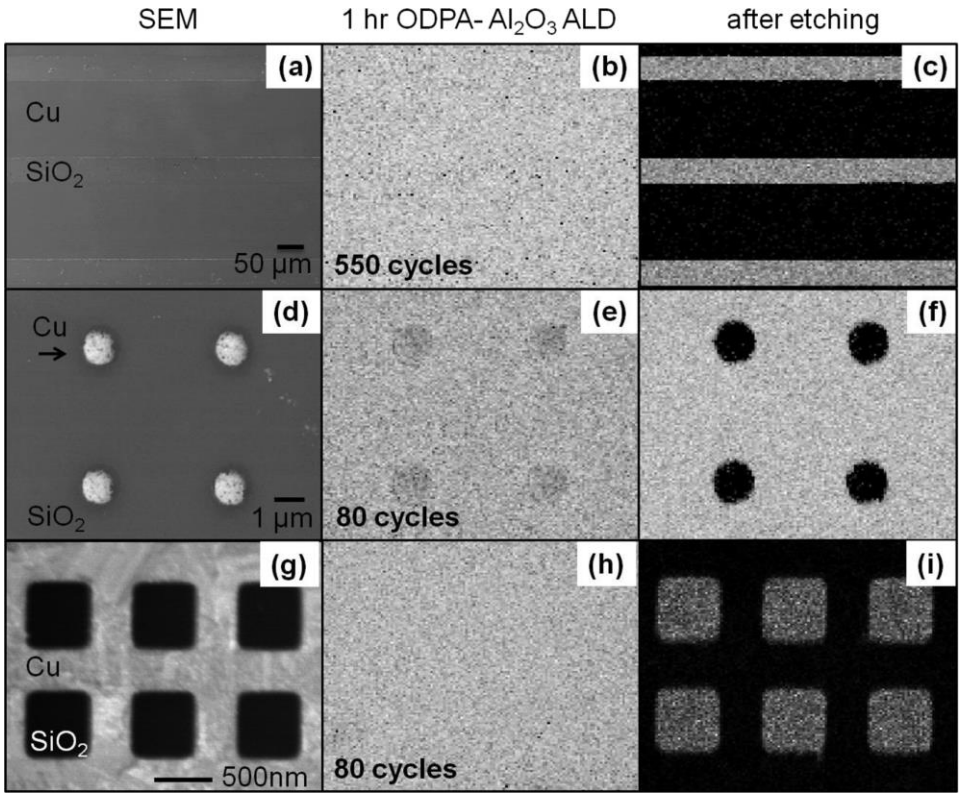

Figure 1. Demonstration of 2-D area selectivity. (a, d, g) Scanning electron microscopy images of patterned Cu/SiO_2 substrates. (b, e, h) Al Auger map of the patterned Cu/SiO_2 substrates treated with octadecylphosphonic acid for 1 h and (b) 250, (e) and (h) 80 cycles of Al_2O_3 ALD. (c, f, i) Al Auger map after the self-correcting etch process is carried out. Figure from Reference [2].

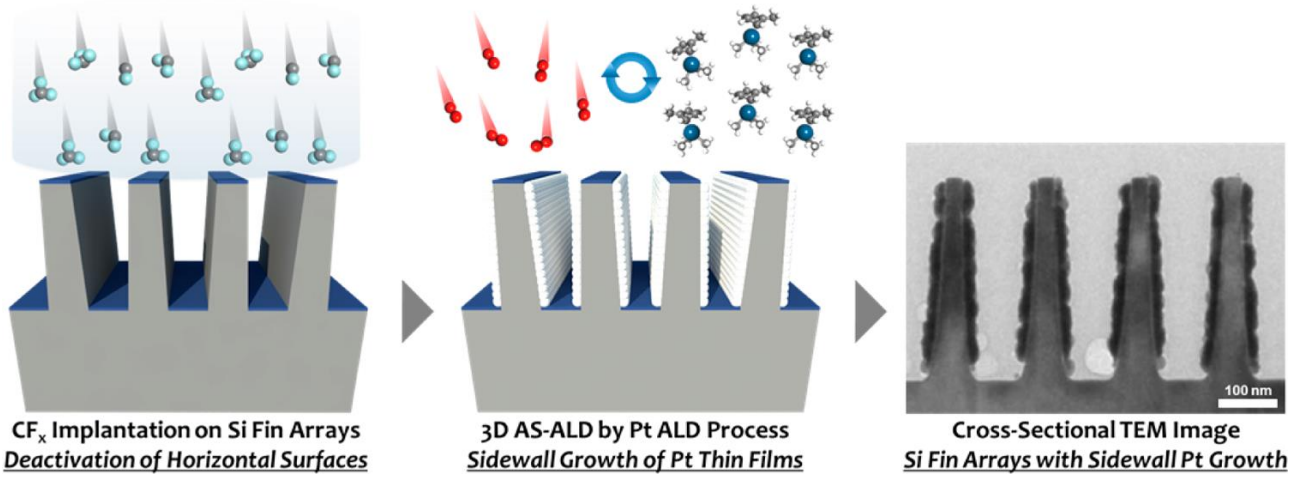

Figure 2. (Left and Center) Schematic of the topographically selective ALD process. (Right) Cross sectional TEM image of a silicon fin array substrate after the process, showing topographical selectivity in which Pt is deposited only on the vertical sidewalls after the horizontal surfaces are blocked by CF_x implantation. Figure from Reference [3].